What Is Claimed Is:

1. A backplane system to connect in common a plurality of peripheral computing devices each on an individual daughter card such that there is a corresponding number of daughter cards, wherein the daughter cards are configured as cPCI-compliant cards each having a slot connector, the backplane system comprising:

a. a backplane bus having a plurality of slots for receiving one or more of the cPCI-compliant cards, wherein said slots are spaced from one another at a pitch to minimize impedance mismatching, each slot including a card connector; and

b. an interposer card for each daughter card, said interposer card including means to connect to the slot connector and to said card connector such that said interposer card is interposed between the daughter card and a slot of said plurality of slots of said backplane bus, wherein said interposer card is designed to convert reflective wave of the daughter card into incident wave switching at said slot connector.

2. The backplane system as claimed in **Claim 1** wherein said backplane bus is a cPCI backplane, the system further comprising a cPCI interface coupled between said backplane bus and the daughter cards, wherein said interposer card is couplable between said cPCI interface and said slot connector of said backplane bus.

3. The backplane system as claimed in **Claim 2** wherein said cPCI interface includes a state machine to regulate timing, direction and enablement associated with operation of said interposer card.

4. The backplane system as claimed in **Claim 3** wherein said state machine and said interposer card are implemented integrally with said interface.

5. The backplane system as claimed in **Claim 1** wherein said interposer card includes a GTLP transceiver to produce incident wave switching.

6. The backplane system as claimed in **Claim 1** wherein said backplane bus has an impedance of about 65 ohms.

7. The backplane system as claimed in **Claim 1** wherein said backplane bus further includes impedance terminations at opposing ends thereof.

8. The backplane system as claimed in **Claim 7** wherein each of said impedance terminations of said backplane has an impedance of about 40 ohms.

9. The backplane system as claimed in **Claim 1** wherein each of said slots includes a stub connector having a stub impedance of about 50 ohms.

10. The backplane system as claimed in **Claim 1** wherein said backplane bus includes 21 of said plurality of slots.

11. A method of increasing the throughput of a conventional cPCI-compliant backplane architecture having a plurality of slots coupled to a common backplane bus for receiving one or more cPCI-compliant daughter cards, the method comprising the step of inserting an interposer card between each of the daughter cards and its corresponding slot, wherein said interposer card includes means for converting reflective-wave switching associated with signal propagation of the daughter card into incident-wave switching at the backplane bus.

12. The method as claimed in **Claim 11** further comprising the step of installing at the ends of the backplane bus termination impedances each having an impedance of about 40 ohms.

13. The method as claimed in **Claim 11** further comprising the step of forming stub connectors of each of the slots with stub impedances of about 50 ohms.

14. The method as claimed in **Claim 11** further comprising the step of coupling said interposer card with a state machine configured to regulate timing, direction, and enablement of said incident-wave switching.

15. The method as claimed in **Claim 11** wherein said interposer card includes a GTLP transceiver for generating said incident-wave switching.

16. The method as claimed in **Claim 11** wherein said backplane bus has an impedance of about 65 ohms.

17. The method as claimed in **Claim 11** further comprising the step of latching the signal transmissions associated with said incident-wave switching so as to control the signal propagation to and from the backplane bus.

18. The method as claimed in **Claim 11** wherein the backplane bus is a cPCI backplane and one or more of the daughter cards is a cPCI-compliant card, further comprising the step of interposing between the cPCI-compliant card and the interposer card a cPCI interface.

19. The method as claimed in **Claim 18** further comprising a state machine formed integrally with said interface, wherein said state machine regulates operation of said interposer card.

20. The method as claimed in **Claim 18** further comprising a state machine formed integrally with said interface, wherein said state machine regulates operation of said interposer card, further comprising the step of forming said interposer card integrally with said interface.